What is Claimed is:

1. A multi-chip memory device, comprising:

at least two integrated circuit memory chips, each of which includes a plurality of corresponding address pads, data pads and control signal pads;

a common package that encapsulates the at least two integrated circuit memory chips and that includes a plurality of external terminals; and

an internal connection circuit in the common package that is configured to connect at least one of the corresponding control signal pads of each of the integrated circuit memory chips to separate ones of the plurality of external terminals to allow independent external control of each of the integrated circuit memory chips that are encapsulated in the common package.

2. A multi-chip memory device according to Claim 1 wherein the at least two integrated circuit memory chips comprise at least two identical integrated circuit memory chips.

3. A multi-chip memory device according to Claim 1 wherein the at least one of the corresponding control circuit pads comprises a chip select signal pad and wherein the internal connection circuit in the common package is configured to connect the chip select signal pad of each of the integrated circuit memory chips to separate ones of the plurality of external terminals to allow independent external chip selection of each of the integrated circuit memory chips that are encapsulated in the common package.

4. A multi-chip memory device according to Claim 1 wherein the at least one of the corresponding control circuit pads comprises a clock enable signal pad and wherein the internal connection circuit in the common package is configured to connect the clock enable signal pad of each of the integrated circuit memory chips to separate ones of the plurality of external terminals to allow independent external clocking of each of the integrated circuit memory chips that are encapsulated in the common package.

5. A multi-chip memory device according to Claim 3 wherein the at least one of the corresponding control circuit pads comprises a clock enable signal pad and

wherein the internal connection circuit in the common package is configured to connect the clock enable signal pad of each of the integrated circuit memory chips to separate ones of the plurality of external terminals to allow independent external clocking of each of the integrated circuit memory chips that are encapsulated in the common package.

6. A multi-chip memory device according to Claim 1 wherein the internal connection circuit in the common package is further configured to connect the corresponding data pads of each of the integrated circuit memory chips in common to a plurality of corresponding external terminals.

7. A multi-chip memory device according to Claim 1 wherein the internal connection circuit in the common package is further configured to separately connect the corresponding data pads of each of the integrated circuit memory chips to separate ones of the external terminals.

8. A multi-chip memory device according to Claim 1 in combination with a memory module substrate including first and second opposing surfaces, wherein the multi-chip memory device is a first multi-chip memory device and is on the first surface, and in further combination with a second multi-chip memory device on the second surface, the second multi-chip memory device comprising:

at least two integrated circuit memory chips, each of which includes a plurality of corresponding address pads, data pads and control signal pads;

a common package that encapsulates the at least two integrated circuit memory chips and that includes a plurality of external terminals; and

an internal connection circuit in the common package that is configured to connect at least one of the corresponding control signal pads of each of the integrated circuit memory chips to separate ones of the plurality of external terminals to allow independent external control of each of the integrated circuit memory chips that are encapsulated in the common package.

9. A multi-chip memory device, comprising:

at least two integrated circuit memory chips, each of which includes a plurality of corresponding address pads, data pads and control signal pads;

a common package that encapsulates the at least two integrated circuit memory chips and that includes a plurality of external terminals; and

means for independently controlling each of the integrated circuit memory chips that are encapsulated in the common package, via at least one of the plurality of external terminals.

10. A multi-chip memory device according to Claim 9 wherein the means for independently controlling comprises an internal connection circuit in the common package that is configured to connect at least one of the corresponding control signal pads of each of the integrated circuit memory chips to separate ones of the plurality of external terminals to allow independent external control of each of the integrated circuit memory chips that are encapsulated in the common package.

11. A memory module comprising:

a memory module substrate including first and second opposing surfaces;

at least one multi-chip memory device on the first surface and on the second surface, each of the multi-chip memory devices comprising:

at least two integrated circuit memory chips, each of which includes a plurality of corresponding address pads, data pads and control signal pads;

a common package that encapsulates the at least two integrated circuit memory chips and that includes a plurality of external terminals; and

an internal connection circuit in the common package that is configured to connect at least one of the corresponding control signal pads of each of the integrated circuit memory chips to separate ones of the plurality of external terminals to allow independent external control of each of the integrated circuit memory chips that are encapsulated in the common package.

12. A memory module according to Claim 11 wherein the at least two integrated circuit memory chips comprise at least two identical integrated circuit memory chips.

13. A memory module according to Claim 11 wherein the at least one of the corresponding control circuit pads comprises a chip select signal pad and wherein the internal connection circuit in the common package is configured to connect the

chip select signal pad of each of the integrated circuit memory chips to separate ones of the plurality of external terminals to allow independent external chip selection of each of the integrated circuit memory chips that are encapsulated in the common package.

14. A memory module according to Claim 11 wherein the at least one of the corresponding control circuit pads comprises a clock enable signal pad and wherein the internal connection circuit in the common package is configured to connect the clock enable signal pad of each of the integrated circuit memory chips to separate ones of the plurality of external terminals to allow independent external clocking of each of the integrated circuit memory chips that are encapsulated in the common package.

15. A memory module according to Claim 11 wherein the internal connection circuit in the common package is further configured to connect the corresponding data pads of each of the integrated circuit memory chips in common to a plurality of corresponding external terminals.

16. A memory module according to Claim 11 wherein the memory module substrate further comprises an external connection circuit that is configured to simultaneously enable only one of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on the first surface and on the second surface.

17. A memory module according to Claim 16 wherein the external connection circuit is further configured to simultaneously enable only a corresponding one of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on the first surface and on the second surface.

18. A memory module according to Claim 16 wherein the external connection circuit is further configured to simultaneously enable only a first of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on the first surface and to simultaneously enable only a second of the

at least two integrated circuit memory chips in each of the at least one multi-chip memory device on the second surface.

19. A memory module according to Claim 16 wherein the external connection circuit is further configured to simultaneously enable only a first of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on a first portion of the first surface and on a corresponding first portion of the second surface and to simultaneously enable a only a second of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on a second portion of the first surface and on a corresponding second portion of the second surface.

20. A memory module according to Claim 16 wherein the external connection circuit further comprises a first external system clock circuit that is configured to provide a first external system clock signal to the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on the first surface and to provide a second external system clock signal to the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on the second surface.

21. A memory module according to Claim 16 wherein the external connection circuit further comprises a first external system clock circuit that is configured to provide a first external system clock signal to the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on a first portion of the first surface and on a corresponding first portion of the second surface, and to provide a second external system clock signal to the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on a second portion of the first surface and on a corresponding second portion of the second surface.

22. A method of controlling a multi-chip memory device that comprises at least two integrated circuit memory chips, each of which includes a plurality of corresponding address pads, data pads and control signal pads and a common package

that encapsulates the at least two integrated circuit memory chips and that includes a plurality of external terminals, the method comprising:

independently controlling each of the integrated circuit memory chips that are encapsulated in the common package, from external of the common package.

23. A method according to Claim 22 wherein the independently controlling comprises independently selecting each of the integrated circuit memory chips that are encapsulated in the common package, from external of the common package.

24. A method according to Claim 22 wherein the independently controlling comprises independently enabling a clock signal for each of the integrated circuit memory chips that are encapsulated in the common package, from external of the common package.

25. A method of controlling a memory module that comprises a memory module substrate including first and second opposing surfaces and at least one multi-chip memory device on the first surface and on the second surface, each of the multi-chip memory devices comprising at least two integrated circuit memory chips, each of which includes a plurality of corresponding address pads, data pads and control signal pads, and a common package that encapsulates the at least two integrated circuit memory chips and that includes a plurality of external terminals, the method comprising:

simultaneously enabling only one of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on the first surface and on the second surface.

26. A method according to Claim 25 wherein the simultaneously enabling comprises simultaneously enabling only a corresponding one of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on the first surface and on the second surface.

27. A method according to Claim 25 wherein the simultaneously enabling comprises simultaneously enabling only a first of the at least two integrated circuit

memory chips in each of the at least one multi-chip memory device on the first surface and to simultaneously enable a only a second of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on the second surface.

28. A method according to Claim 25 wherein the simultaneously enabling comprises simultaneously enabling only a first of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device on a first portion of the first surface and a corresponding first portion of the second surface and to simultaneously enable a only a second of the at least two integrated circuit memory chips in each of the at least one multi-chip memory device a second portion of the first surface and on a corresponding second portion of the second surface.